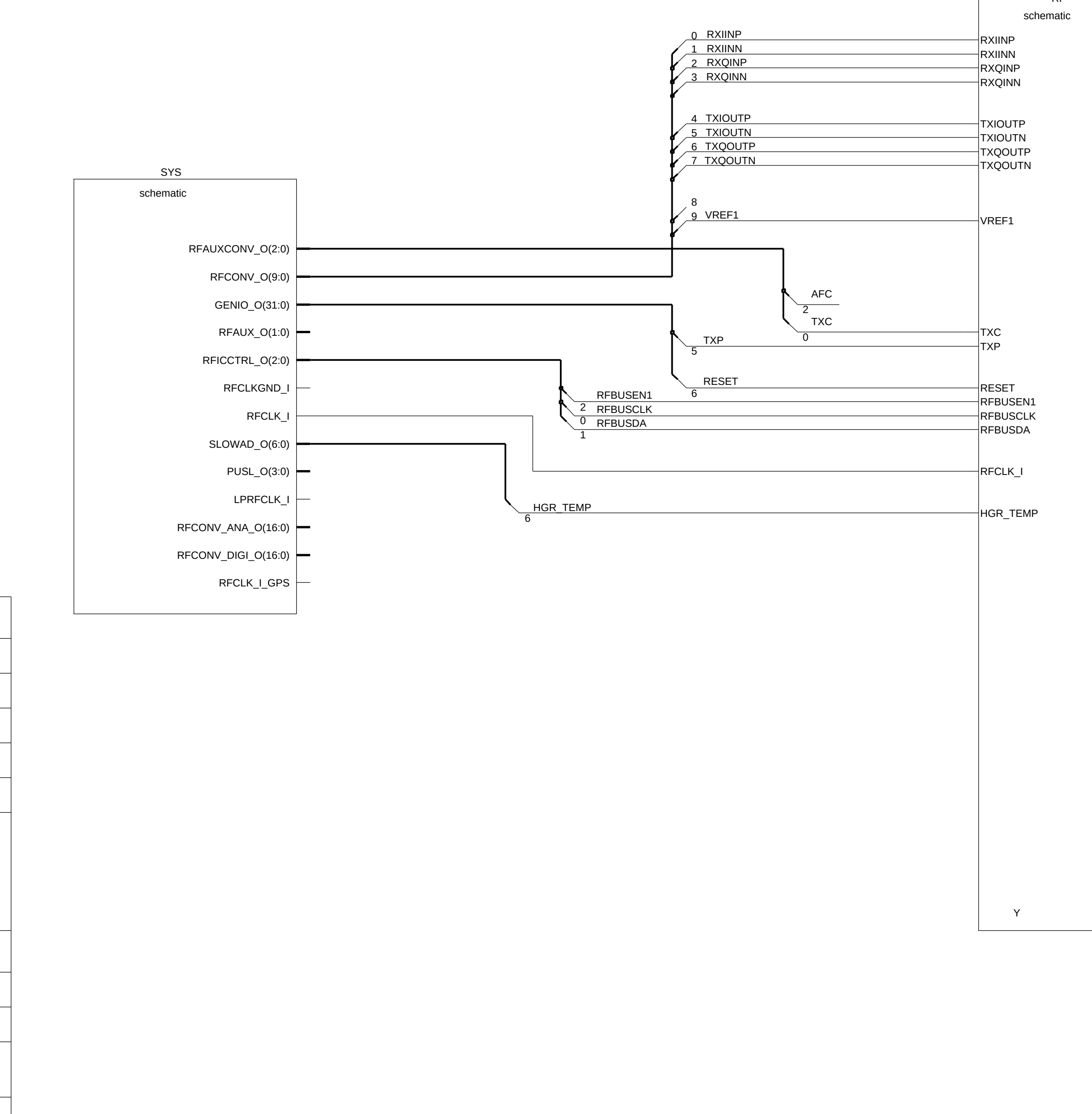
8 - SCHEMATICS

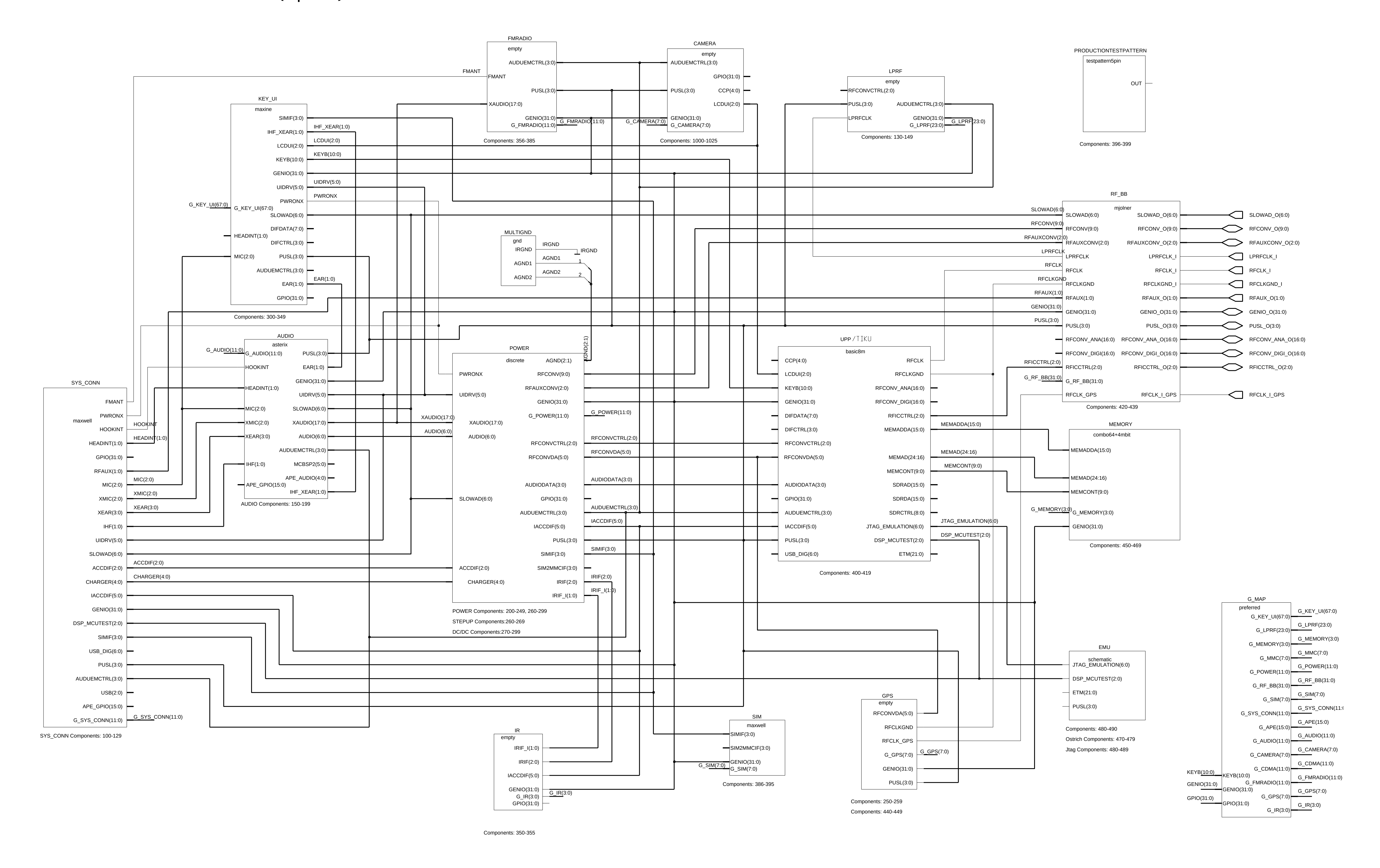
Table of Contents

Title: Top Sheet

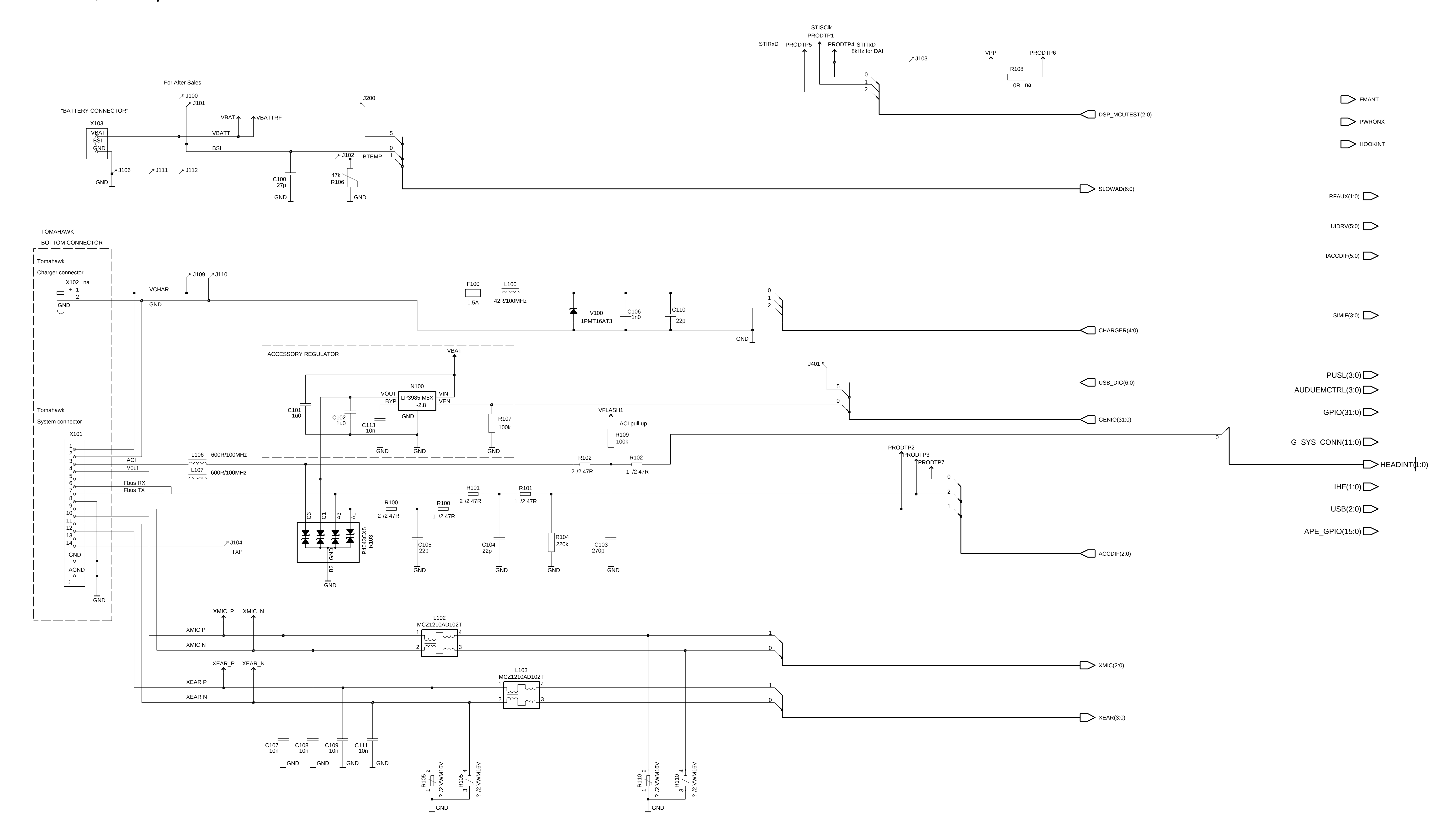


CBB _OVERVIEW		MODEL	CBB_VERSION
SYS_CONN		MAXWELL	SYS_6.1
KEY_UI		MAXINE	SYS_6.1
AUDIO		MAXWELL	SYS_6.1
FMRADIO		EMPTY	SYS_6.1
MULTIGND		GND	SYS_6.1
POWER		DISCRETE	SYS_6.1
	PWRFILTER	LIGHT	SYS_6.1
	DC_DC	EMPTY	SYS_6.1
	REG_CAP	MAXWELL	SYS_6.1
	PWR_RES	THERM1	SYS_6.1
IR		EMPTY	SYS_6.1
CAMERA		EMPTY	SYS_6.1
LPRF		EMPTY	SYS_6.1
UPP		BASIC8M	SYS_6.1
	UPPFILTER	DISCRETE	SYS_6.1
SIM		MAXWELL	SYS_6.1
GPS		EMPTY	SYS_6.1
PRODUCTIONSPATTERN		TESTPATTERN 5PIN	SYS_6.1
	MODULE_ID	MODULE_ID	SYS_6.1
RF_BB		MJOLNER	SYS_6.1
MEMORY		COMBO64+4MBIT	SYS_6.1
	MEMFILTER	NOVFLASH1CAP	SYS_6.1
	MEMWING	EMPTY	SYS_6.1
	MEMEXTENSION	EMPTY	SYS_6.1
EMU		SCHEMATIC	SYS_6.1
	JTAG	TESTPOINT	SYS_6.1
	OSTRICH	TESTPOINT	SYS_6.1
	ETM	EMPTY	SYS_6.1

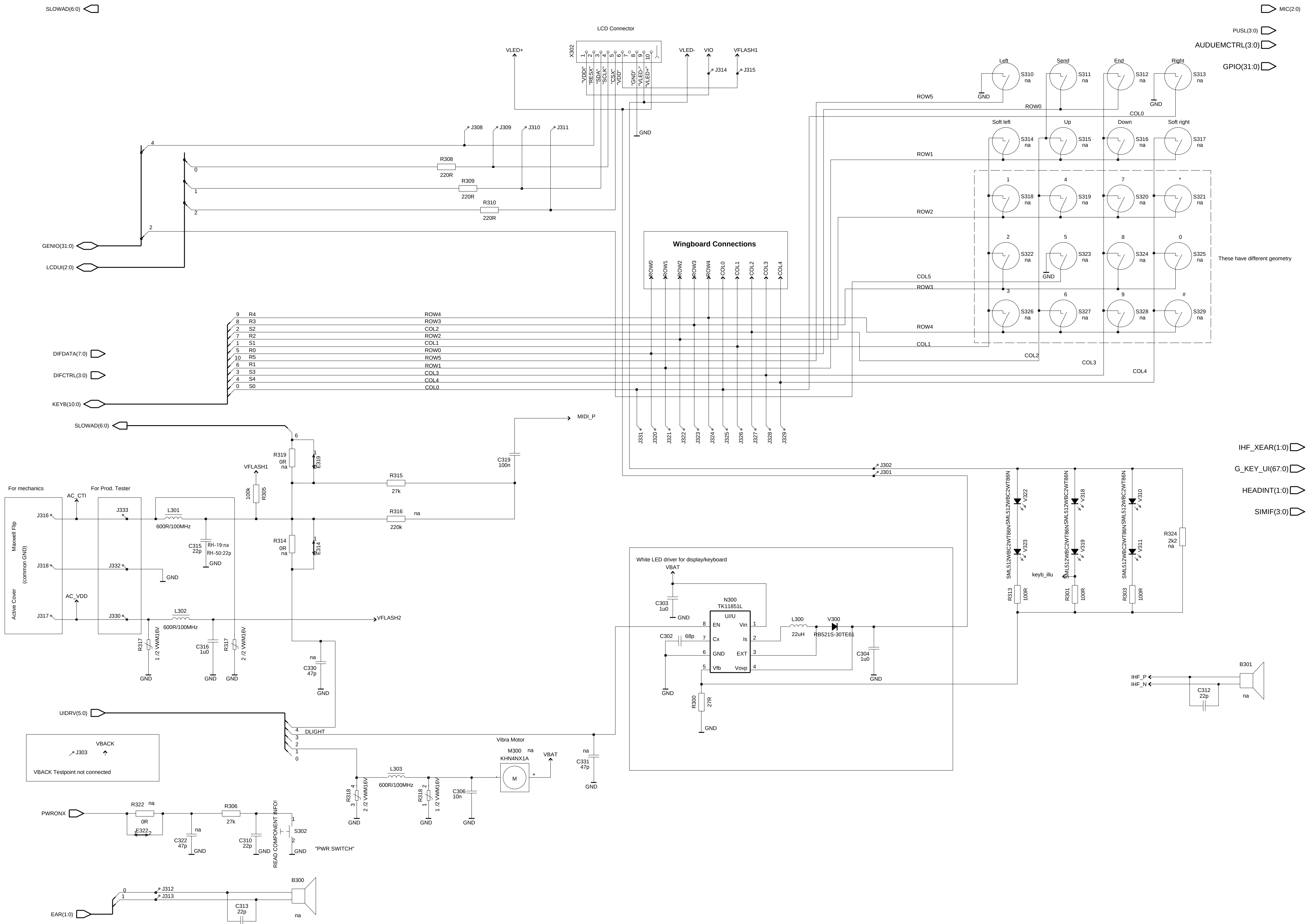
Title: DCT4 Common Baseband Schematic (Top Level)



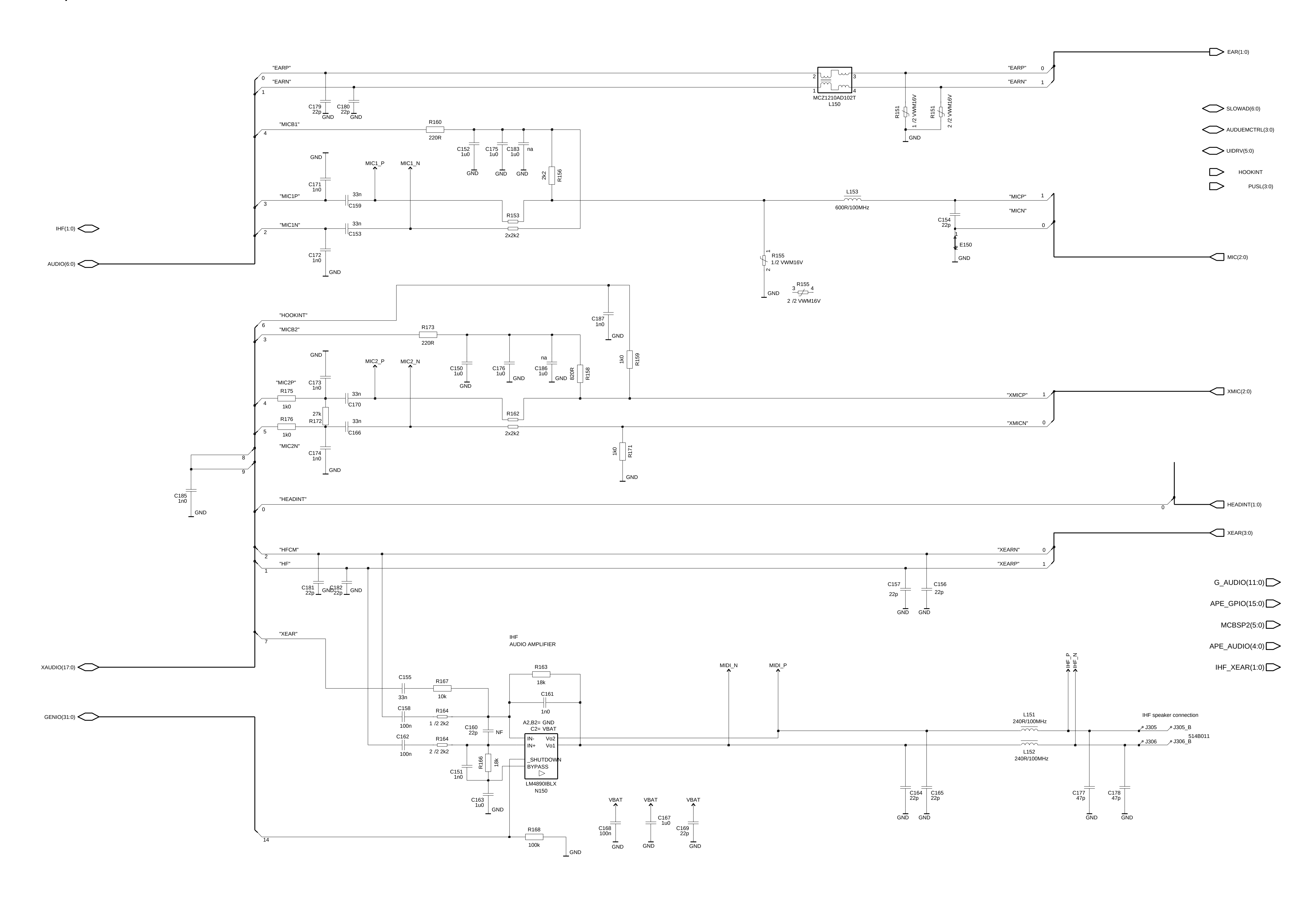
Title: RH-19/RH-50 System Connector



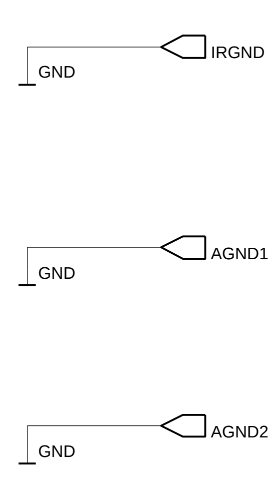
Title: RH-19/RH-50 User Interface



Title: RH-19/RH-50 Audio

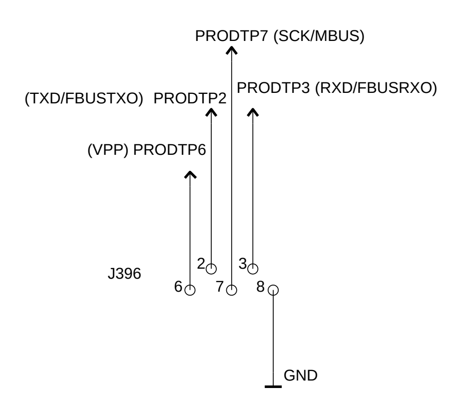


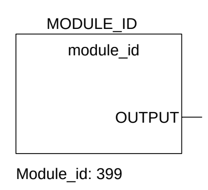
Title: MultiGND Synbol Bypass



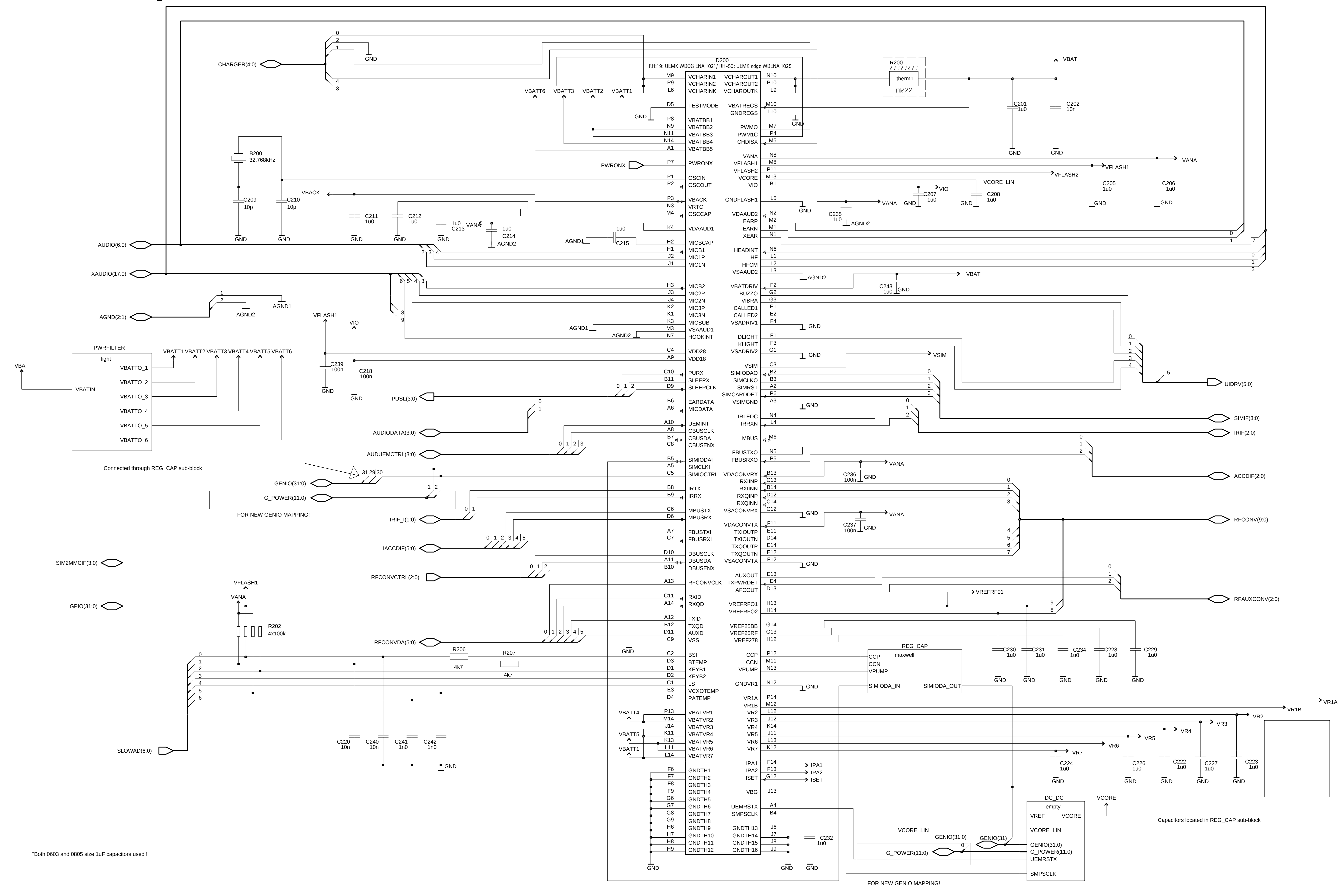
Title: 5 pin Production Test Pattern

OUT

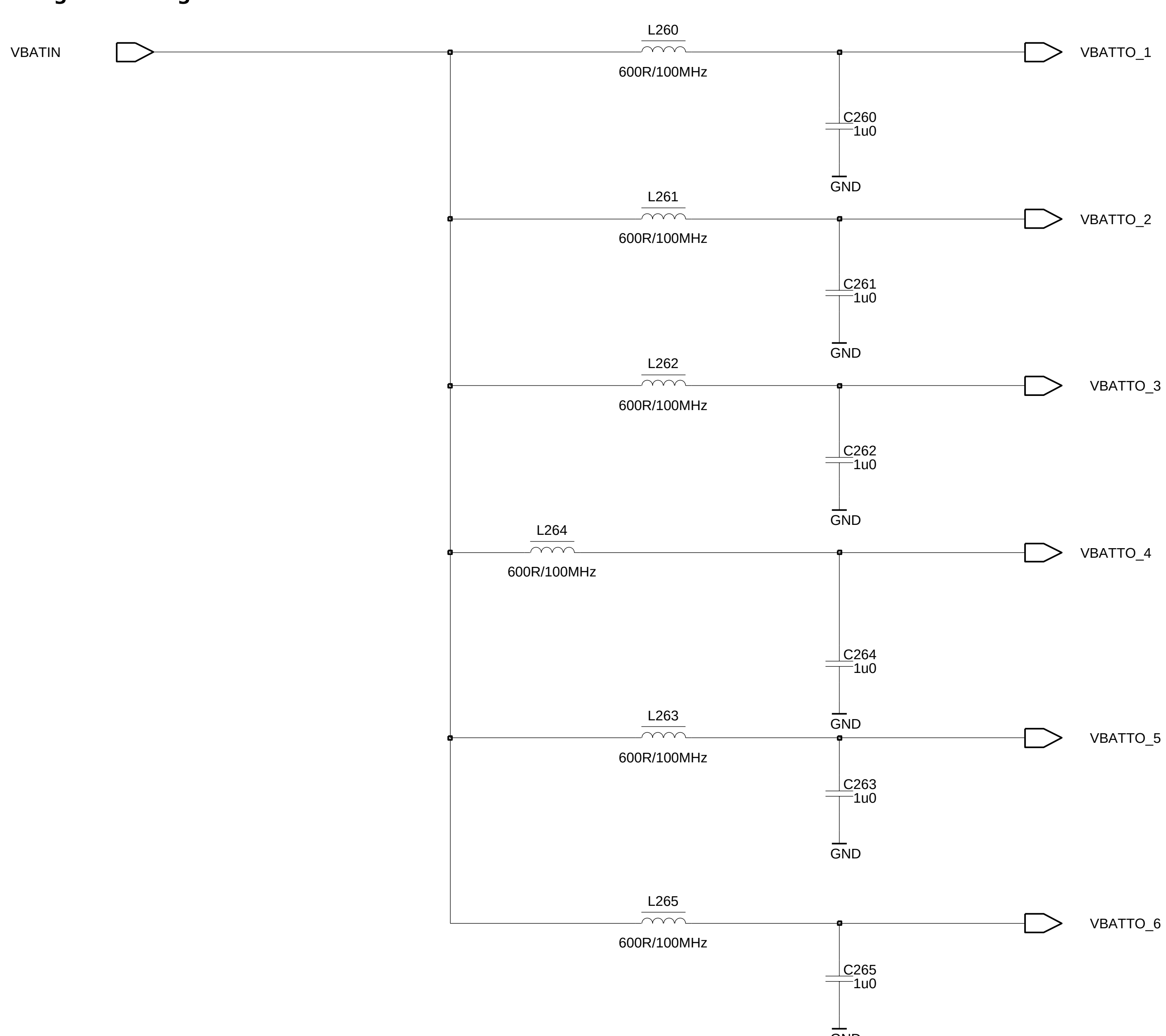




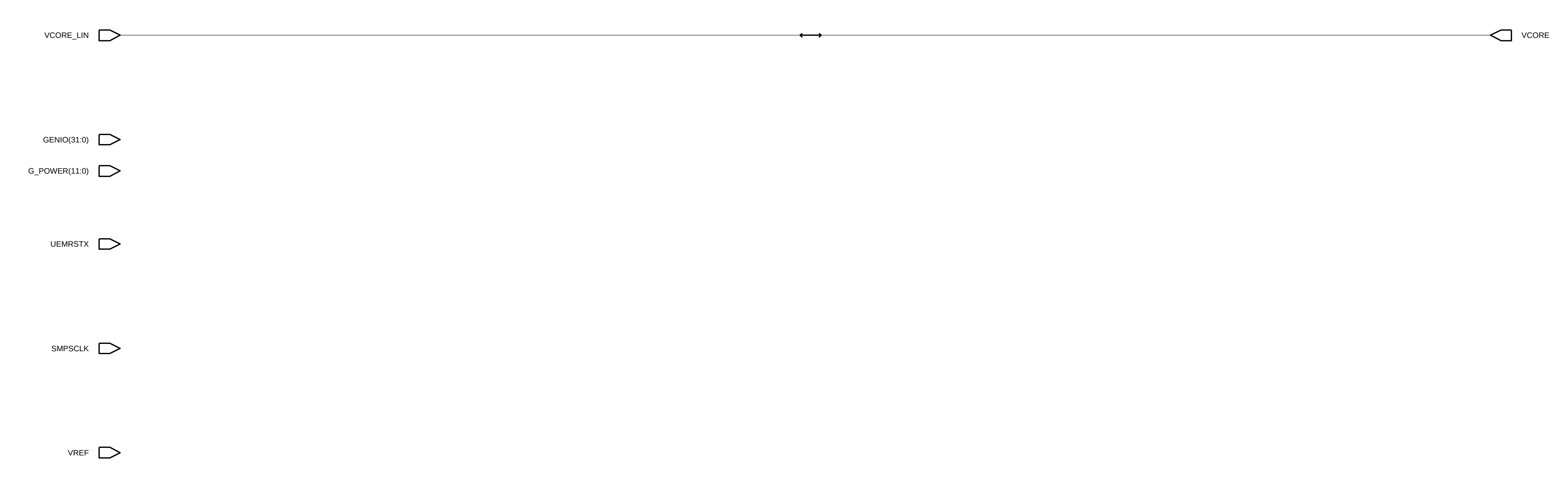
Title: Discrete Power Management



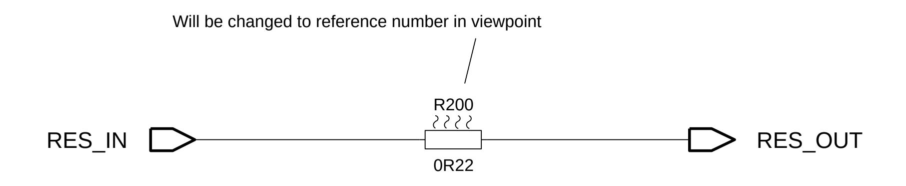
Title: Light Filtering



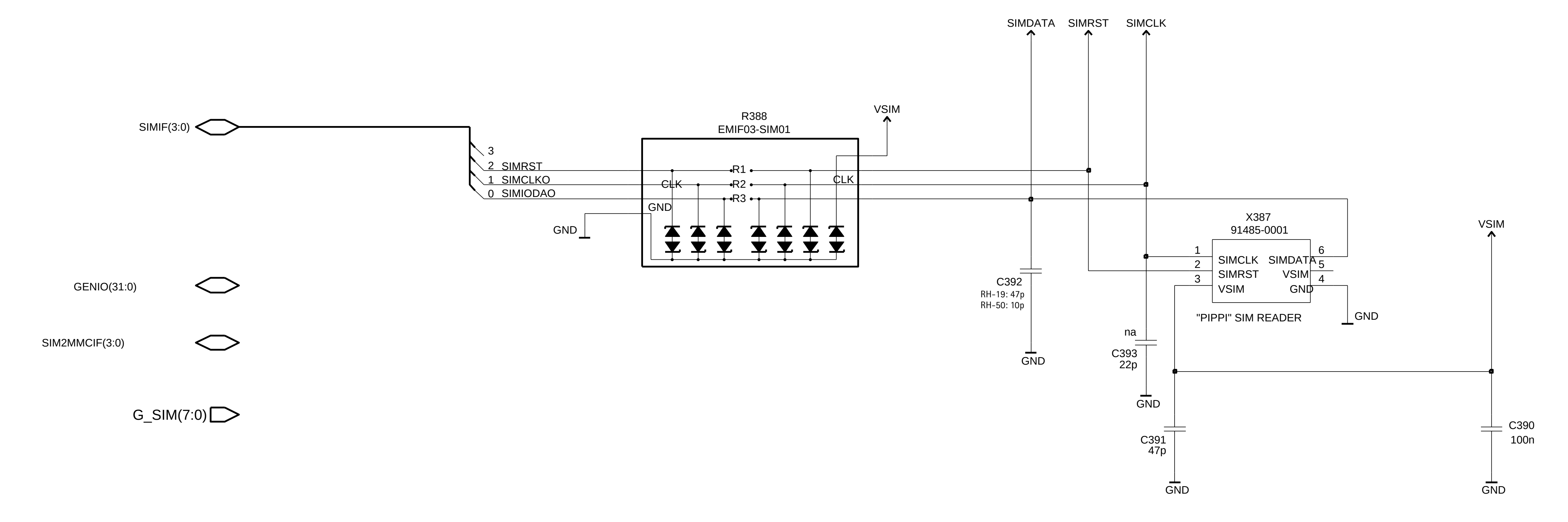
Title: DC/DC Convertor



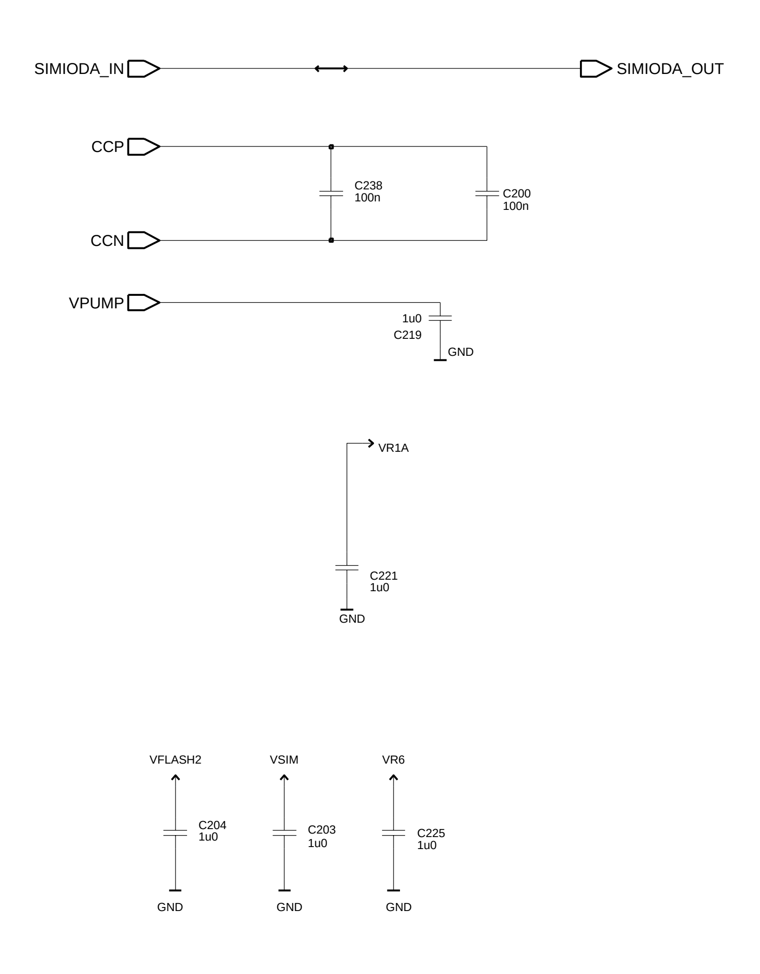
Title: PWR Resistor 0805 thermal1



Title: SIM Reader for RH-19/RH-50



Title: RH-19/RH-50 Filters / No IR Interface present in this project



IACCDIF(5:0)

1

GND

UPP input
is grounded, when IR
is not used!

GENIO(31:0)

GPIO(31:0)

IRIF(2:0)

2

GND

UEM IR level shifters
are ground, when IR
is not used!

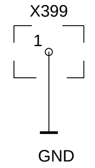
IRIF_I(1:0)

0

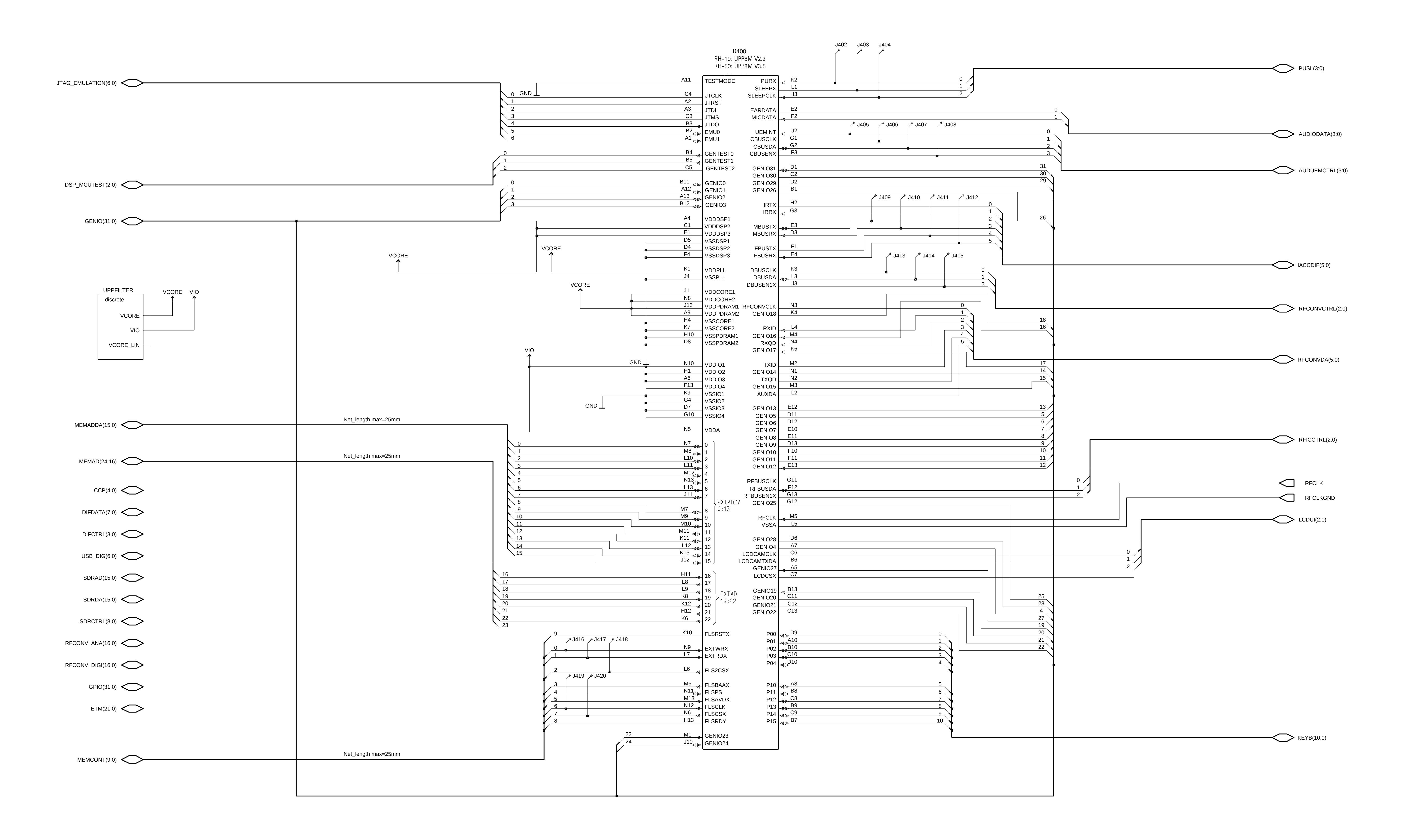
GND

Title: Module ID

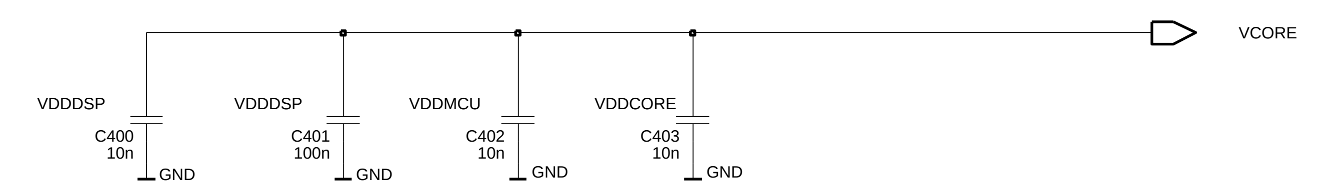
OUTPUT



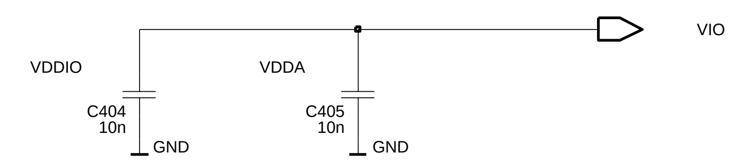
Title: UPP 8M Implementation



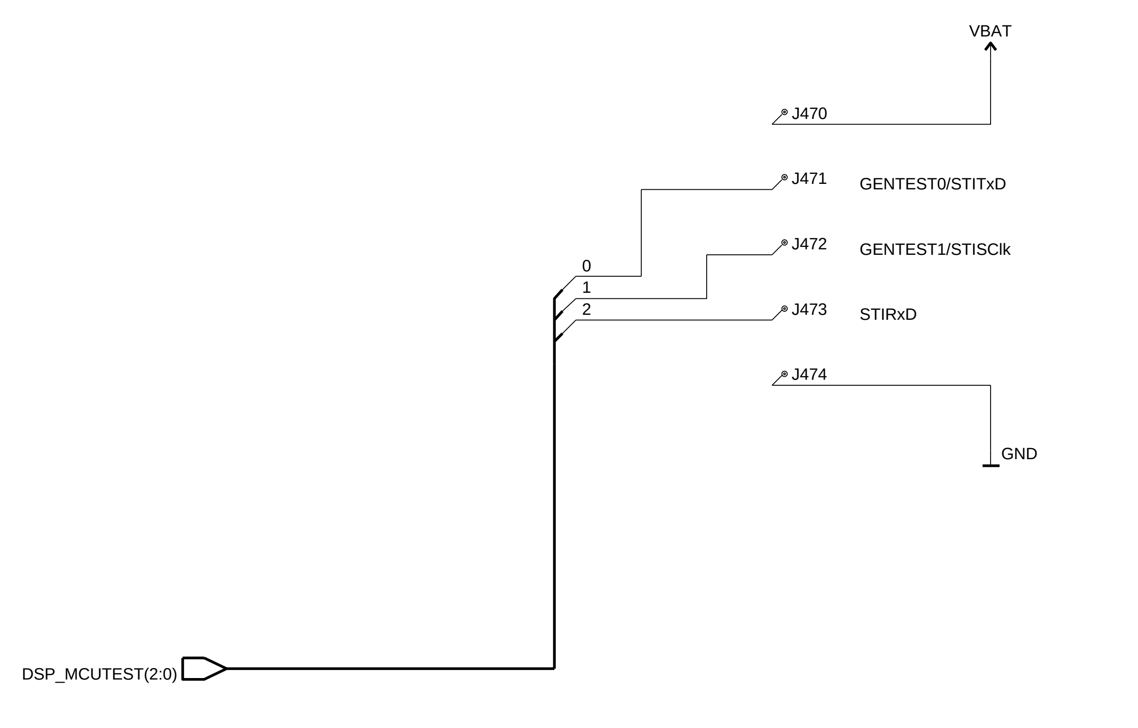
Title: Discrete Decoupling Capacitors for UPP



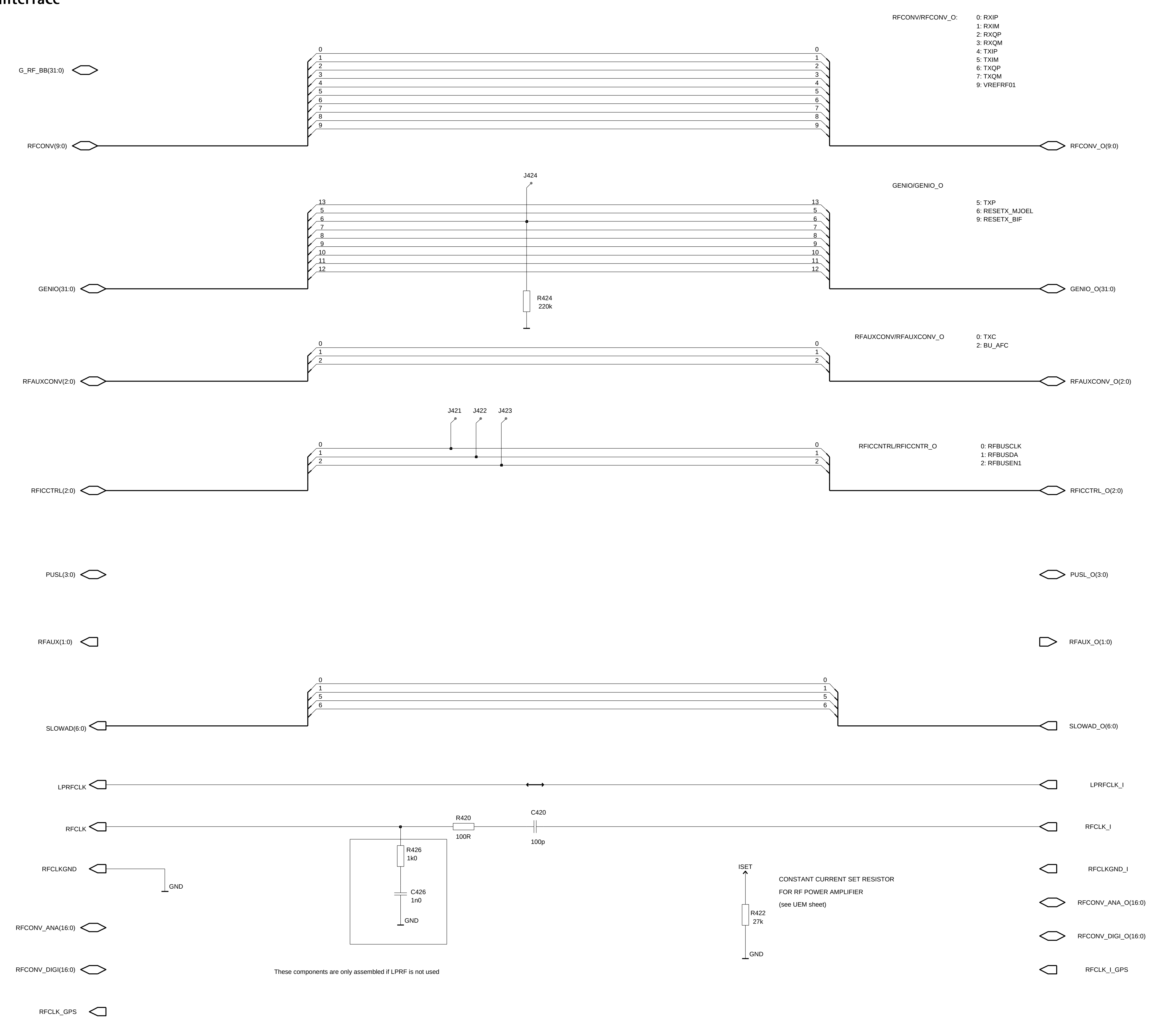
VCORE_LIN



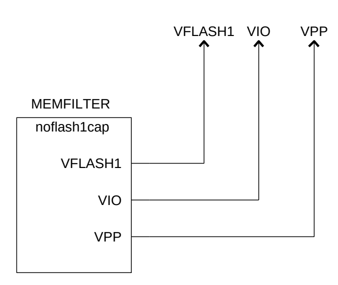
Title: Testpoints based Ostrich Inteface



Title: GSM RF - Baseband Interface



Title: Combo Memory 64 + 4 Mbit



MEMEXTENSION
empty
MEMADDA(15:0)
MEMAD(24:16)
MEMCONT(9:0)
GENIO(31:0)
G_MEMORY(3:0)
FLS2CSX

MEMWING
empty
GENIO(31:0)
G_MEMORY(3:0)
MEMAD(24:16)
MEMADDA(15:0) FLS2CSX
MEMCONT(9:0) FLSCSX

GENIO(31:0) 23

D450
K5U64418TM-TD90
FLASHM 4Mx16
SRAM 256kx16

MEMAD(16) B2 16
MEMAD(17) A9
MEMAD(18) B8 A
MEMAD(19) A8
MEMAD(20) B3 20
FLASH/SRAM
MEMAD(21) A2 A21/_LB
MEMAD(22) A10 A22/_UB
B7 _WP/_CS
FLASH
MEMCONT(6) A4 CLK RDY A1
MEMCONT(9) B6 _RESET
B9 _CEF
NC 1 E451
NC 2 E452
NC 3 E453
COMMON NC 4 E454
MEMCONT(5) B4 _AVD NC 5 E455
MEMCONT(0) A6 _WE NC 6 E456
MEMCONT(1) C10 _OE NC 7 E457
MEMCONT(4) B5 PS NC 8 E458

D10
ADDRESS/DATA I/O
0 D9
1 C7
2 C6
3 D5
4 D4
5 C3
6 C2
7 C9
8 C8
9 D7
10 D6
11 C5
12 C4
13 D2
14 D1
15

VPP PRODTP6
MEMCONT(3) R450 4k7 E450 2

MEMAD(24:16)
MEMCONT(9:0) MEMCONT(8)

A5,B1,D8= VIO
A7= VPP
A3,B10,C1,D3= GND

MEMADDA(15:0)

G_MEMORY(3:0)

Title: Discrete Capacitors for Memory without VFlash1







Title: Empty Wing Sheet

MEMADDA(15:0)

MEMAD(24:16)

GENIO(31:0)

G_MEMORY(3:0)

FLS2CSX

2

7

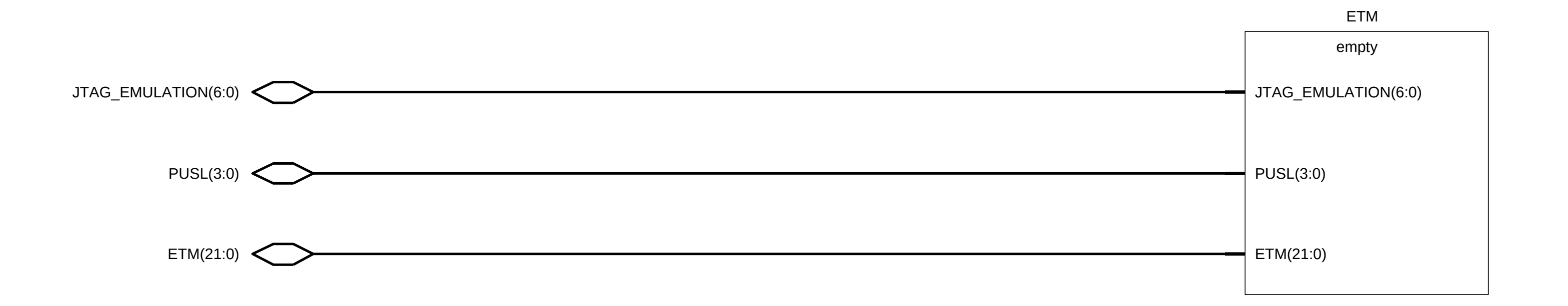
FLSCSX

MEMCONT(9:0)

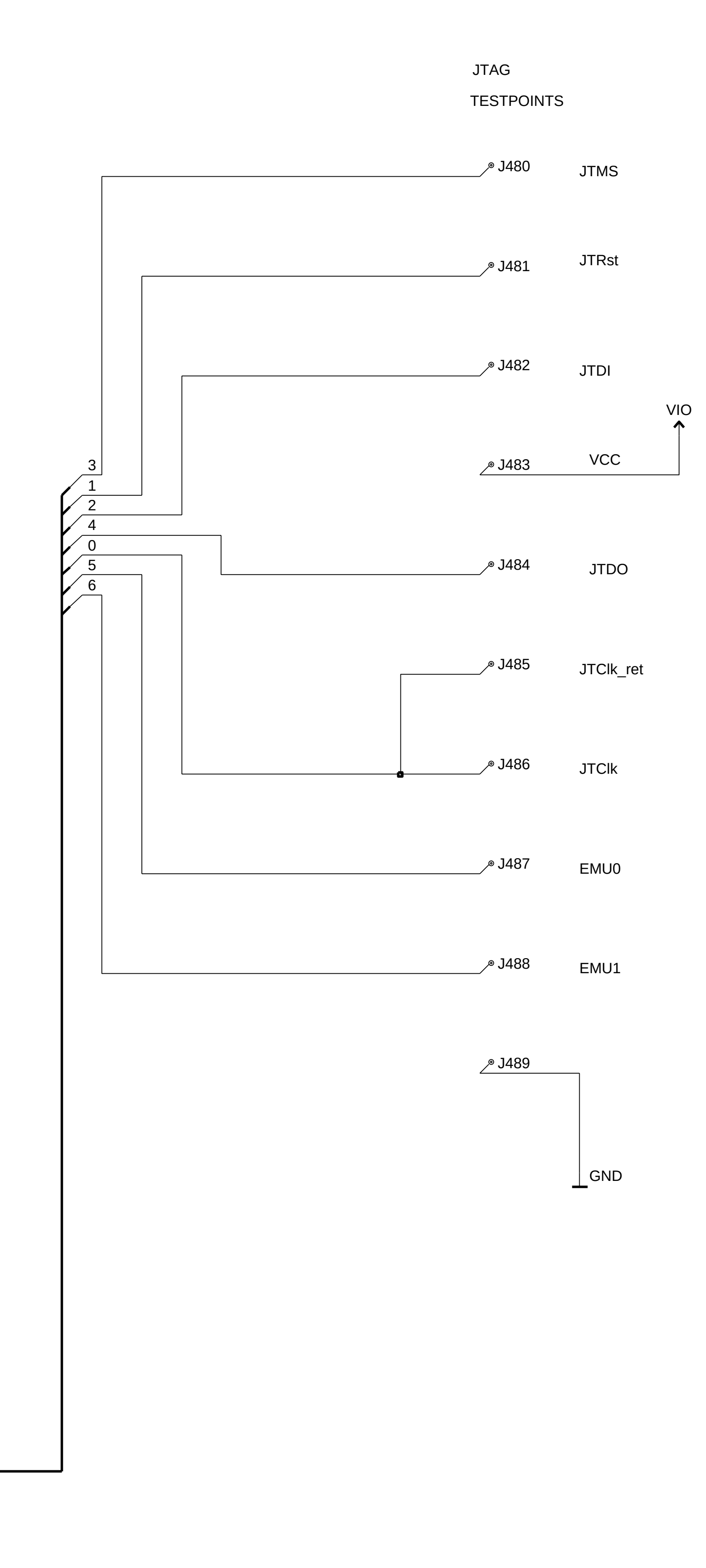
Title: Test and Emulator Inteface



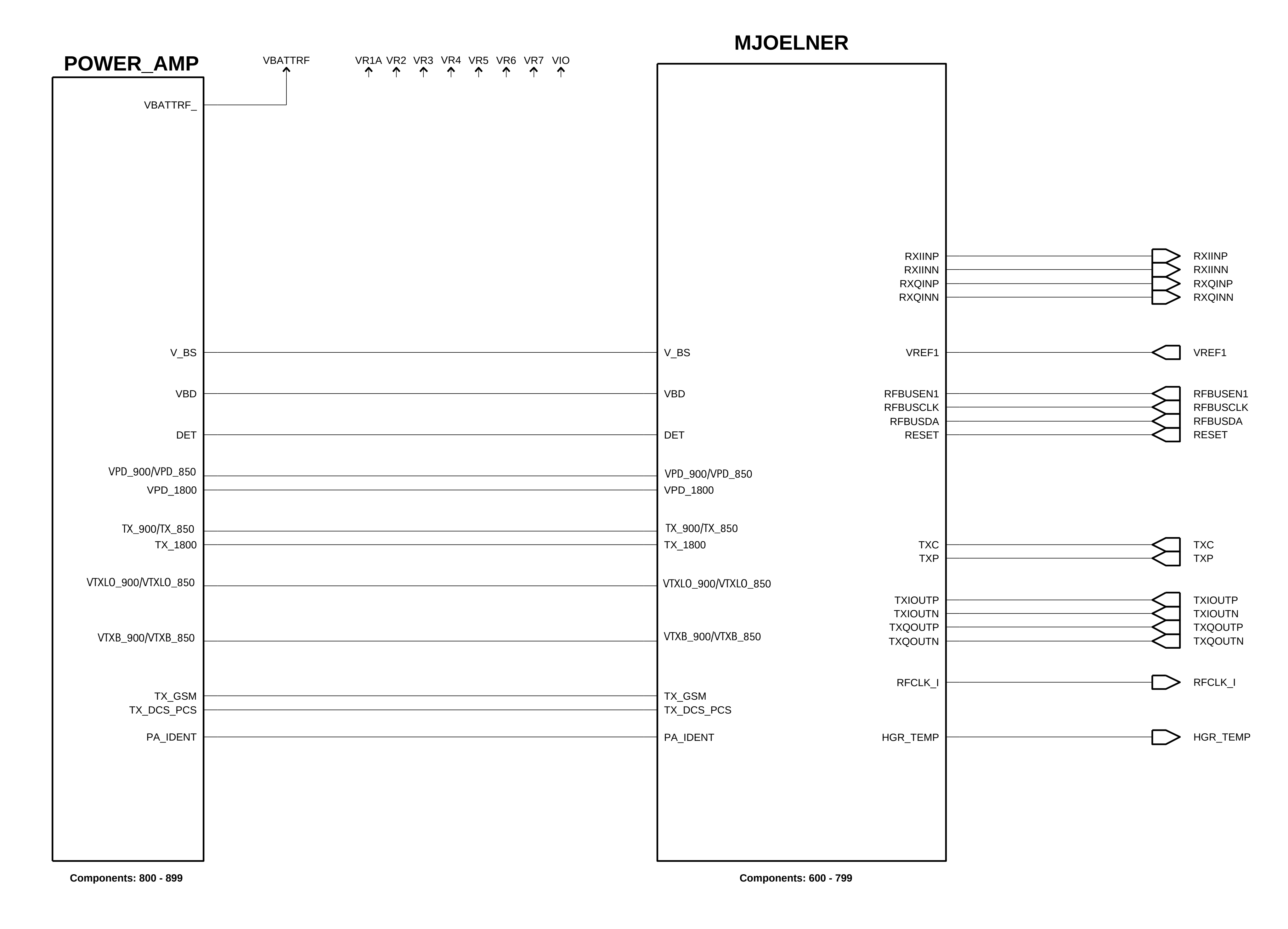




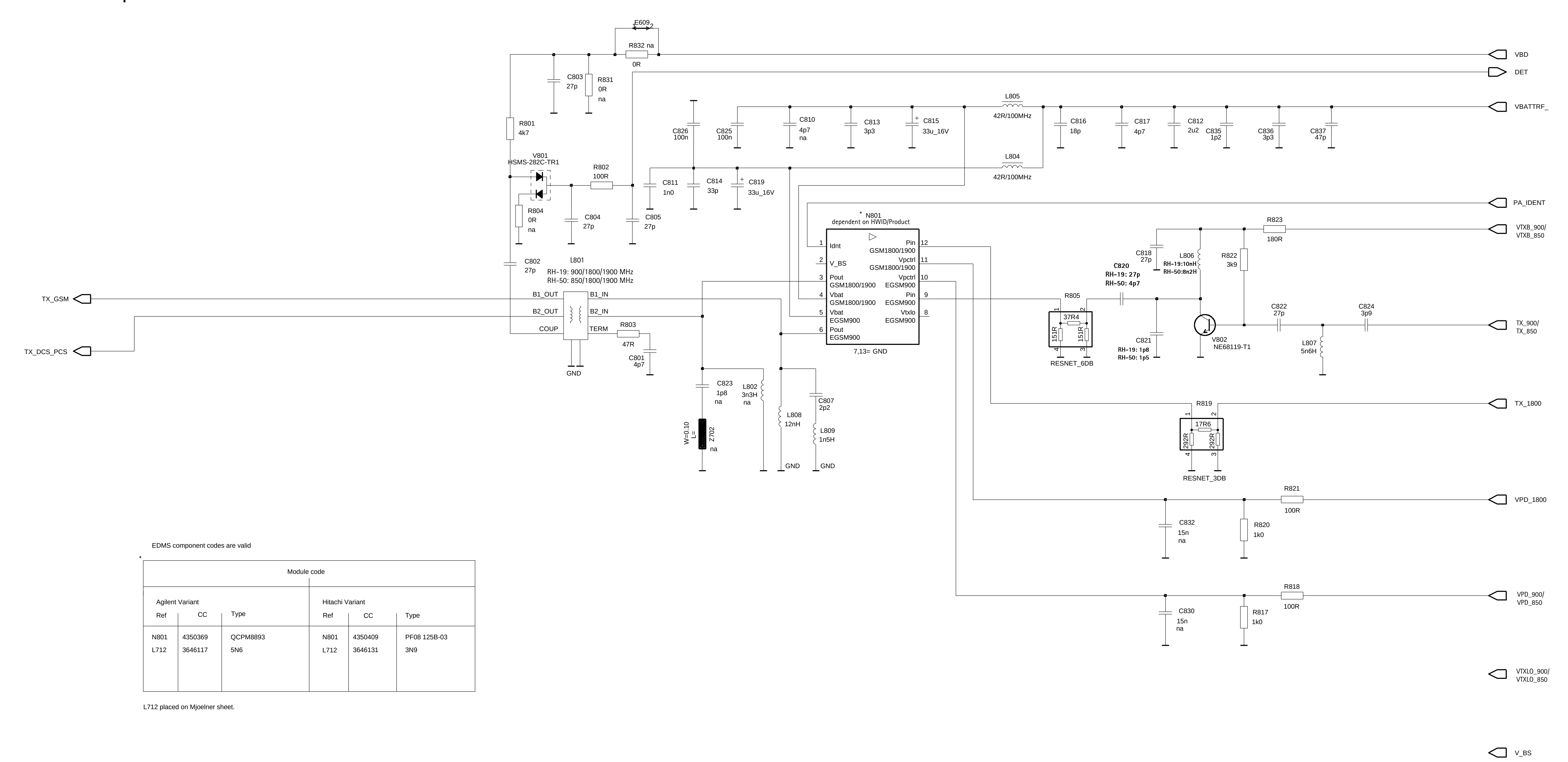
Title: Testpoints for JTAG Emulator



Title: RF Top Sheet

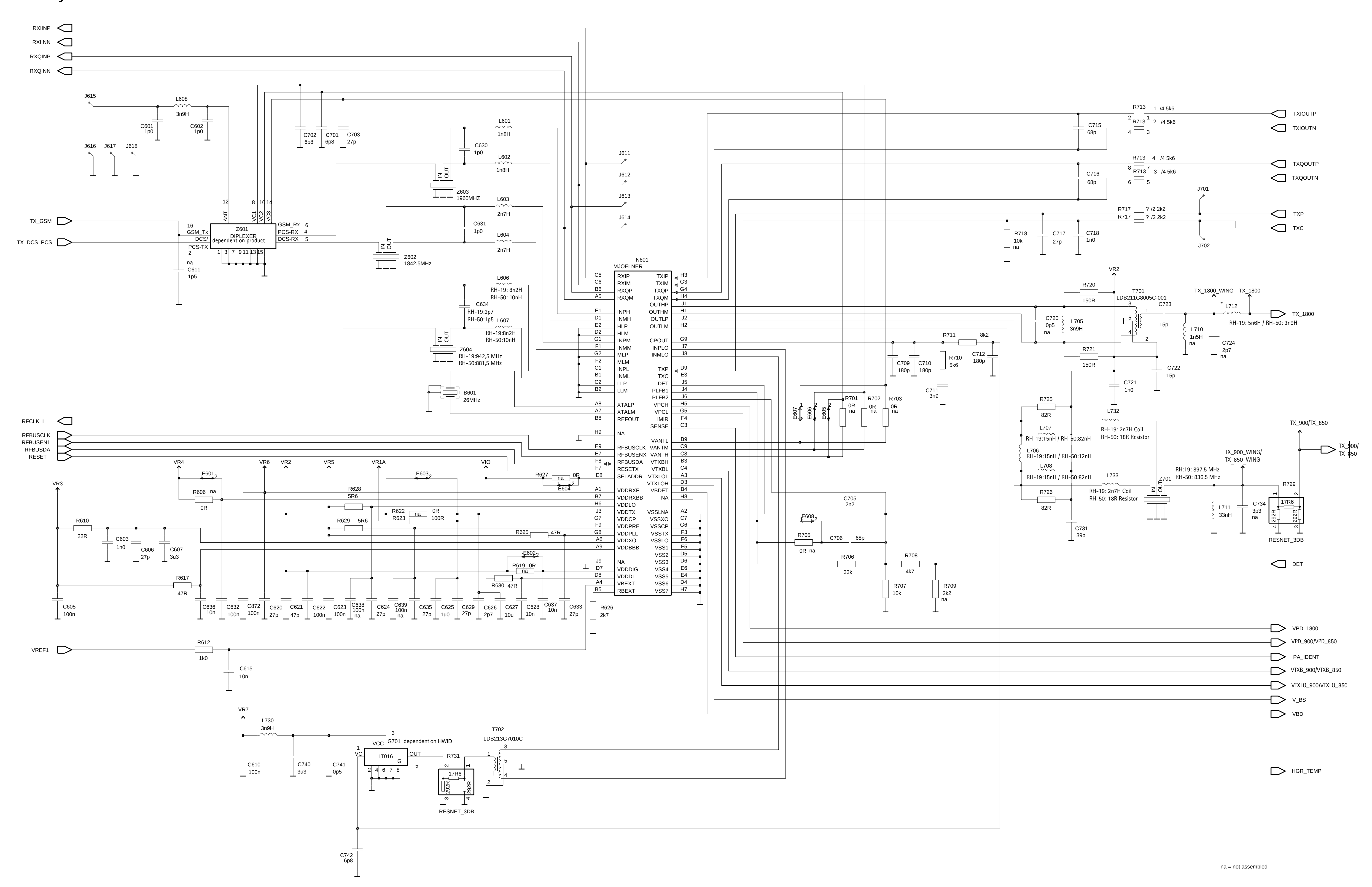


Title: Power Amplifier

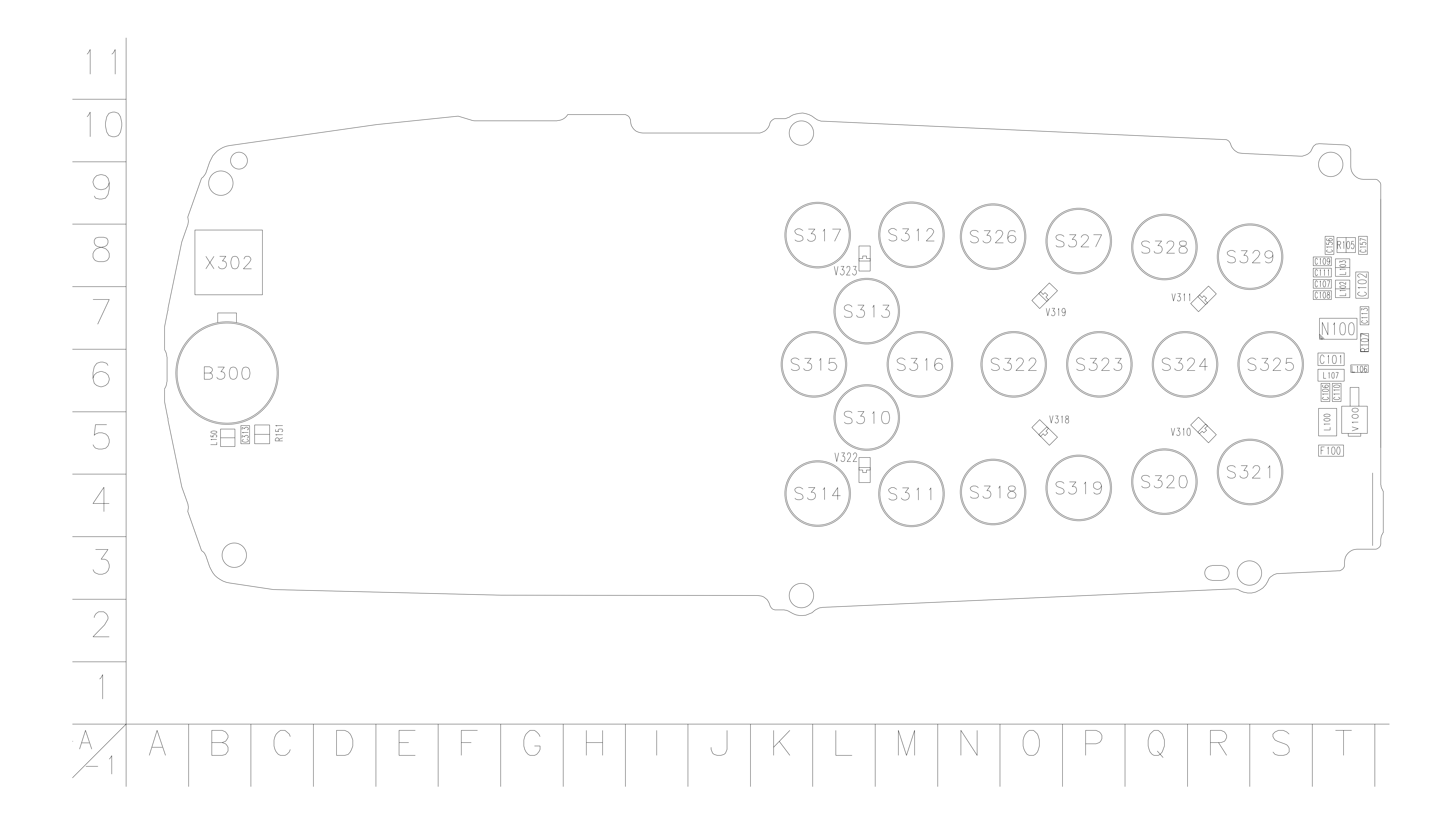


Module code					
Agilent Variant			Hitachi Variant		
Ref	CC	Type	Ref	CC	Type
N801	4350369	QCPM8893	N801	4350409	PF08 125B-03
L712	3646117	5N6	L712	3646131	3N9

Title: Mjoelner



Component layout diagram, top



Component layout diagram, bottom

